

IN THE CLAIMS:

- 1 | 1. (currently amended) ~~In a voltage-controlled oscillator (VCO) defining a feedback~~
2 | ~~loop that~~ A buffer circuit that generates an output signal to control the frequency of a
3 | VCO, with a frequency responsive to an input control signal, the VCO further the buffer
4 | circuit comprising:
5 | a control FET transistor, defining a threshold voltage V_t , a gate, source and drain,
6 | where the control signal is connected to the gate,
7 | a means for receiving at least a portion of the current from the drain of the control
8 | FET, wherein the current is responsive to the input control signal, wherein the current
9 | controls the frequency of the output signal,
10 | a bipolar diode connected to receive the current from the source of the control
11 | FET, wherein the diode compensates for temperature effects of the control FET, and
12 | a resistor in parallel with the bipolar diode.
- 1 | 2. (canceled)
- 1 | 3. (currently amended) The VCO of claim 1 wherein the diode comprises an NPN base
2 | emitter, and further the buffer circuit having an ~~and a~~ PNP base emitter arranged as a di-
3 | ode in parallel with each other the NPN base emitter and with the collectors of the NPN
4 | and the PNP connected to their respective bases.
- 1 | 4. (currently amended) The ~~VCO~~ buffer circuit of claim 1 further comprising:
2 | a second FET, configured with its gate connected to its drain,
3 | the second FET drain connected to the drain of the first FET wherein the current
4 | through the second FET is in ~~parallel to~~ series with the current through the first FET.
- 1 | 5. (currently amended) The ~~VCO~~ Vbuffer circuit of claim 4 wherein both the first and
2 | second FET's are N type MOSFETS.

1 6. (canceled)

1 7. (currently amended) The buffer circuit ~~The VCO~~ of claim 1 wherein the means for
2 receiving the drain current from the first FET comprises a diode connected ~~fourth~~ FET.

1 8. (currently amended) The buffer circuit ~~The VCO~~ of claim 7 further comprising a
2 ~~fifth~~ mirror FET connected as a current mirror to the ~~fourth~~ diode connected FET of
3 claim 7, wherein the current from the mirror FET is also used to control the output signal
4 frequency.

1 9. (currently amended) ~~In a voltage controlled oscillator (VCO) defining a feedback~~
2 ~~loop that~~ A buffer circuit that generates an output signal to control the frequency of a
3 VCO, with a frequency responsive to an input control signal, the VCO further the buffer
4 circuit comprising:
5 an a first N type MOSFET with its gate connected to the control input signal,
6 a resistor connected to receive the source current from the first N type MOSFET,
7 a bipolar NPN diode connected transistor and a bipolar PNP diode connected
8 transistor both connected in parallel with each other and with the resistor and arranged to
9 receive the current from the source of the first N type MOSFET,
10 a diode connected P type MOSFET arranged with its drain connected to the drain
11 of the first N type MOSFET transistor and arranged to receive the current from the drain
12 of the first N type MOSFET,
13 second and third diode connected N type MOSFET transistors in series with each
14 other and connected to and arranged to draw current from the drain of the P type MOS-
15 FET, and
16 a second P type MOSFET connected a s a current mirror with the first P type
17 MOSFET transistor, wherein the currents through the first and the second P type MOS-
18 FET's control the output signal frequency.

1 | 10. (currently amended) The buffer circuit ~~The VCO~~ of claim 9 wherein the currents
2 | through the first and the second P type MOSFET transistors ~~follows~~ follow a square law
3 | relationship with respect to the input control signal.